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IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 4. (Cancelled)

5. (Currently Amended) A semiconductor integrated circuit ~~according to Claim 1~~, wherein:

a buffer circuit from which the true and a complementary signal are output based upon input signals and a decoder circuit for decoding based upon signals output from said buffer circuit are provided;

a semiconductor logic circuit in which at least one of said buffer circuit and said decoder circuit is controlled for precharge and evaluation operation according to the polarity of a control signal input to its control terminal and the true and a complementary signal are output based upon input signals input to its input terminals is provided;

said semiconductor logic circuit of said decoder circuit is composed of a set in which an output signal including said true of any of plural said buffer circuits is input to its control terminal and a set to which a complementary output signal is input, and output signals from the other buffer circuits are input to the input terminal of said semiconductor logic circuit of said decoder circuit; and

said semiconductor logic circuit comprises:

a first load provided between a first power source terminal and a first node and controlled by said control signal and a second load provided between said first power source terminal and a second node and controlled by said control signal;

a logic circuit for input provided between said first node and a third node for electrically connecting said first node and said third node according to said input signal;

a field effect transistor for reference paths to the source and the drain of which are provided between said second node and said third node and the gate of which is connected to said first node; and

an activation circuit provided between said third node and a second power source terminal and controlled by said control signal.

6. (Original) A semiconductor integrated circuit according to Claim 5, wherein:

said semiconductor logic circuit comprises:

a first field effect transistor for feedback paths to the source and the drain of which are provided between said first node and said logic circuit for input and the gate of which is connected to said second node; and

a second field effect transistor for feedback paths to the source and the drain of which are provided between said second node and said field effect transistor for reference and the gate of which is connected to said first node.

7. (Original) A semiconductor integrated circuit according to Claim 5, wherein:

in said semiconductor logic circuit, the terminal of said logic circuit for input connected to said third node is connected to said second power source terminal, said load is controlled by a first control signal and said activation circuit is controlled by a second control signal.

8. – 9. (Cancelled)

10. (Currently Amended) A semiconductor logic circuit ~~according to Claim 8~~, wherein:

a first load provided between a first power source terminal and a first node and controlled by a control signal and a second load provided with said first power source terminal and a second node and controlled by said control signal;

a logic circuit for input provided between said first node and a third node for electrically connecting said first node and said third node according to an input signal;

a field effect transistor for reference paths to the source and the drain of which are provided between said second node and said third node and the gate of which is connected to said first node; and

an activation circuit provided between said third node and a second power source terminal and controlled by said control signal, wherein:

a reset circuit for reducing the pulse length of a signal output from said semiconductor logic circuit is provided;

said reset circuit is composed of at least either of the following first or second reset circuit:

a first reset circuit, one terminal of which is connected to said first node and the other terminal of which is connected to a fourth node for reducing the pulse length of said fourth node by a first reset signal; and

a second reset circuit, one terminal of which is connected to said second node and the other terminal of which is connected to a fifth node for reducing the pulse length of said fifth node by a second reset signal.

11. (Cancelled)

12. (Currently Amended) A semiconductor logic circuit ~~according to Claim 8~~, wherein:

a first load provided between a first power source terminal and a first node and controlled by a control signal and a second load provided with said first power source terminal and a second node and controlled by said control signal;

a logic circuit for input provided between said first node and a third node for electrically connecting said first node and said third node according to an input signal;

a field effect transistor for reference paths to the source and the drain of which are provided between said second node and said third node and the gate of which is connected to said first node;

an activation circuit provided between said third node and a second power source terminal and controlled by said control signal, wherein:

a reset circuit for reducing the pulse length of a signal output from said semiconductor logic circuit is provided; and

said reset circuit comprises:

at least either of a first field effect transistor for reset paths to the source and the drain of which are provided between said first power source terminal and said first node and the gate of which is controlled by a reset pulse or a second field effect transistor for reset paths to the source and the drain of which are provided between said first power source terminal and said second node and the gate of which is controlled by said reset pulse; and

a field effect transistor for preventing a through state paths to the source and the drain of which are provided between said activation circuit and said second power source terminal and the gate of which is controlled by said reset pulse.

13. – 14. (Cancelled)

15. (Original) A semiconductor logic circuit according to Claim 10, wherein:

said each reset circuit comprises:

a field effect transistor paths to the source and the drain of which are provided between said one terminal and said other terminal and the gate of which is connected to said first power source terminal; and

a field effect transistor for precharge paths to the source and the drain of which are provided between said first power source terminal and said other terminal and the gate of which is controlled by said control signal.

16. (Cancelled)

17. (Original) A semiconductor logic circuit according to Claim 10, wherein:

said reset circuit is composed of the combination of the reset circuits according to Claim 13.

18. – 19. (Cancelled)

20. (Currently Amended) A semiconductor logic circuit ~~according to Claim 8~~, wherein:

a first load provided between a first power source terminal and a first node and controlled by a control signal and a second load provided with said first power source terminal and a second node and controlled by said control signal;

a logic circuit for input provided between said first node and a third node for electrically connecting said first node and said third node according to an input signal;

a field effect transistor for reference paths to the source and the drain of which are provided between said second node and said third node and the gate of which is connected to said first node;

an activation circuit provided between said third node and a second power source terminal and controlled by said control signal, wherein:

a reset circuit for reducing the pulse length of a signal output from said semiconductor logic circuit is provided; and

said logic circuit for input is provided with a first input signal and a second input signal and is composed of a first field effect transistor to the gate of which said

first input signal is input and a second field effect transistor to the gate of which said second input signal is input, the drain of which is connected to the drain of said first field effect transistor and the source of which is connected to the source of said first field effect transistor; and

the source is connected to the source of said field effect transistor for reference.

21. (Currently Amended) A semiconductor logic circuit ~~according to Claim 8~~, wherein:

a first load provided between a first power source terminal and a first node and controlled by a control signal and a second load provided with said first power source terminal and a second node and controlled by said control signal;

a logic circuit for input provided between said first node and a third node for electrically connecting said first node and said third node according to an input signal;

a field effect transistor for reference paths to the source and the drain of which are provided between said second node and said third node and the gate of which is connected to said first node;

an activation circuit provided between said third node and a second power source terminal and controlled by said control signal, wherein:

a reset circuit for reducing the pulse length of a signal output from said semiconductor logic circuit is provided; and

said logic circuit for input is acquired by connecting a set of two field effect transistors each gate of which is controlled by each input signal and is cascaded and

a set of two field effect transistors each gate of which is controlled by a complementary input signal of said each input signal and is cascaded in parallel.

22. (Currently Amended) A semiconductor logic circuit ~~according to Claim 8~~, wherein:

a first load provided between a first power source terminal and a first node and controlled by a control signal and a second load provided with said first power source terminal and a second node and controlled by said control signal;

a logic circuit for input provided between said first node and a third node for electrically connecting said first node and said third node according to an input signal;

a field effect transistor for reference paths to the source and the drain of which are provided between said second node and said third node and the gate of which is connected to said first node;

an activation circuit provided between said third node and a second power source terminal and controlled by said control signal, wherein:

a reset circuit for reducing the pulse length of a signal output from said semiconductor logic circuit is provided; and

the number of columns of said field effect transistors for reference is n (n: 2 or integer larger than 2) which is the same as the number of columns of field effect transistors in said logic circuit for input.

23. (Currently Amended) A semiconductor logic circuit ~~according to Claim 8~~, wherein;

a first load provided between a first power source terminal and a first node and controlled by a control signal and a second load provided with said first power source terminal and a second node and controlled by said control signal;

a logic circuit for input provided between said first node and a third node for electrically connecting said first node and said third node according to an input signal;

a field effect transistor for reference paths to the source and the drain of which are provided between said second node and said third node and the gate of which is connected to said first node;

an activation circuit provided between said third node and a second power source terminal and controlled by said control signal, wherein:

a reset circuit for reducing the pulse length of a signal output from said semiconductor logic circuit is provided; and

a selection circuit for supplying an input signal to the input terminal of said logic circuit for input is provided; and

said selection circuit is controlled by a selector signal so that it becomes a selected state or an unselected state, outputs a signal based upon a signal input to said selection circuit in a selected state and keeps the output at the electric potential of said second power source terminal in an unselected state or keeps the output at electric potential immediately before said circuit becomes an unselected state.

24. (Cancelled)

25. (Currently Amended) A semiconductor logic circuit ~~according to Claim 8~~, wherein:

a first load provided between a first power source terminal and a first node and controlled by a control signal and a second load provided with said first power source terminal and a second node and controlled by said control signal;

a logic circuit for input provided between said first node and a third node for electrically connecting said first node and said third node according to an input signal;

a field effect transistor for reference paths to the source and the drain of which are provided between said second node and said third node and the gate of which is connected to said first node;

an activation circuit provided between said third node and a second power source terminal and controlled by said control signal, wherein:

a reset circuit for reducing the pulse length of a signal output from said semiconductor logic circuit is provided; and

said activation circuit is composed of inverters; and the input terminal is controlled by said control signal and the output terminal is connected to said third node.

26. (Currently Amended) A semiconductor logic circuit ~~according to Claim 8~~, wherein:

a first load provided between a first power source terminal and a first node and controlled by a control signal and a second load provided with said first power source terminal and a second node and controlled by said control signal;

a logic circuit for input provided between said first node and a third node for electrically connecting said first node and said third node according to an input signal;

a field effect transistor for reference paths to the source and the drain of which are provided between said second node and said third node and the gate of which is connected to said first node;

an activation circuit provided between said third node and a second power source terminal and controlled by said control signal, wherein:

a reset circuit for reducing the pulse length of a signal output from said semiconductor logic circuit is provided;

said activation circuit is composed of a logic circuit having plural inputs; and

any of the plural inputs is said control signal and the output is connected to said third node.

27. (Cancelled)

28. (Currently Amended) A semiconductor integrated circuit ~~according to Claim 1~~, wherein:

a buffer circuit from which the true and a complementary signal are output based upon input signals and a decoder circuit for decoding based upon signals output from said buffer circuit are provided;

a semiconductor logic circuit in which at least one of said buffer circuit and said decoder circuit is controlled for precharge and evaluation operation according to the polarity of a control signal input to its control terminal and the true and a

complementary signal are output based upon input signals input to its input terminals is provided;

said semiconductor logic circuit of said decoder circuit is composed of a set in which an output signal including said true of any of plural said buffer circuits is input to its control terminal and a set to which a complementary output signal is input, and output signals from the other buffer circuits are input to the input terminal of said semiconductor logic circuit of said decoder circuit; and

said semiconductor logic circuit is composed of ~~said~~a semiconductor logic circuit ~~according to Claim 8~~comprising:

a first load provided between a first power source terminal and a first node and controlled by a control signal and a second load provided with said first power source terminal and a second node and controlled by said control signal;

a logic circuit for input provided between said first node and a third node for electrically connecting said first node and said third node according to an input signal;

a field effect transistor for reference paths to the source and the drain of which are provided between said second node and said third node and the gate of which is connected to said first node; and

an activation circuit provided between said third node and a second power source terminal and controlled by said control signal, wherein:

a reset circuit for reducing the pulse length of a signal output from said semiconductor logic circuit is provided.